CLAIMS

What is claimed is:

1) A triple redundant latch for reducing soft errors comprising:

a) an input driver, the input driver having an input and an output;

b) a first transfer gate, the first transfer gate having an input, a first control input, a second control input and an output;

c) a second transfer gate, the second transfer gate having an input, a first control input, a second control input, and an output;

d) a third transfer gate, the transfer third gate having an input, a first control input, a second control input, and an output;

e) a first feedback inverter, the first feedback inverter having an input and an output;

f) a second feedback inverter, the second feedback inverter having an input and an output;

g) a third feedback inverter, the third feedback inverter having an input and an output;

h) a forward inverter/majority voter, the forward inverter/majority voter having a first input, a second input, a third input and an output;

i) an output driver, the output driver having an input and an output;

j) wherein the input of the input driver is the input of the triple redundant latch;

k) wherein the output of the input driver is connected to the input of the first transfer gate, the input of the second transfer gate, and the input of the third transfer gate;

l) wherein a first control input of the triple redundant latch is connected to the first control input of the first transfer gate, the first control input of the second transfer gate, and the first control input of the third transfer gate;

m) wherein a second control input of the triple redundant latch is connected to the second control input of the first transfer gate, the second control input of the second transfer gate, and the second control input of the third transfer gate;

n) wherein the output of the first transfer gate is connected to the output of the first feedback inverter and to the first input of the forward inverter/majority voter;

o) wherein the output of the second transfer gate is connected to the output of the second feedback inverter and to the second input of the forward inverter/majority voter;

p) wherein the output of the third transfer gate is connected to the output of the third feedback inverter and to the third input of the forward inverter/majority voter;

q) wherein the output of the forward inverter/majority voter is connected to the input of the first feedback inverter, the input of the second feedback inverter, the input of the third feedback inverter, and to the input of the output driver;

r) wherein the output of the output driver is the output of the triple redundant latch.

2) The triple redundant latch as in Claim 1 wherein input driver comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the source of the PFET is connected to VDD;

d) wherein the source of the NFET is connected to GND;

e) wherein the gates of the NFET and the PFET are the input of the input driver;

f) wherein the drains of the NFET and the PFET are the output of the input driver.

3) The triple redundant latch as in Claim 1 wherein the first transfer gate comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the drains of the PFET and the NFET are connected to the input of the first transfer gate;

d) wherein the sources of the PFET and the NFET are connected to the output of the first transfer gate;

e) wherein the gate of the NFET is connected to the first control input of the first transfer gate;

f) wherein the gate of the PFET is connected to the second control input of the first transfer gate.

4) The triple redundant latch as in Claim 1 wherein the second transfer gate comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the drains of the PFET and the NFET are connected to the input of the second transfer gate;

d) wherein the sources of the PFET and the NFET are connected to the output of the second transfer gate;

e) wherein the gate of the NFET is connected to the first control input of the second transfer gate;

f) wherein the gate of the PFET is connected to the second control input of the second transfer gate.

5) The triple redundant latch as in Claim 1 wherein the third transfer gate comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the drains of the PFET and the NFET are connected to the input of the third transfer gate;

d) wherein the sources of the PFET and the NFET are connected to the output of the third transfer gate;

e) wherein the gate of the NFET is connected to the first control input of the third transfer gate;

f) wherein the gate of the PFET is connected to the second control input of the third transfer gate.

6) The triple redundant latch as in Claim 1 wherein the first feedback inverter comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the source of the PFET is connected to VDD;

d) wherein the source of the NFET is connected to GND;

e) wherein the gate of the NFET and the gate of the PFET are the input of the first feedback inverter;

f) wherein the drain of the NFET and the drain of the PFET are the output of the first feedback inverter.

7) The triple redundant latch as in Claim 1 wherein the second feedback inverter comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the source of the PFET is connected to VDD;

d) wherein the source of the NFET is connected to GND;

e) wherein the gate of the NFET and the gate of the PFET are the input of the second feedback inverter;

f) wherein the drain of the NFET and the drain of the PFET are the output of the second feedback inverter.

8) The triple redundant latch as in Claim 1 wherein the third feedback inverter comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the source of the PFET is connected to VDD;

d) wherein the source of the NFET is connected to GND;

e) wherein the gate of the NFET and the gate of the PFET are the input of the third feedback inverter;

f) wherein the drain of the NFET and the drain of the PFET are the output of the third feedback inverter.

9) The triple redundant latch as in Claim 1 wherein the forward inverter/majority voter comprises:

a) a first PFET, the first PFET having a gate, a drain and a source;

b) a second PFET, the second PFET having a gate, a drain and a source;

c) a third PFET, the third PFET having a gate, a drain and a source;

d) a fourth PFET, the fourth PFET having a gate, a drain and a source;

e) a fifth PFET, the fifth PFET having a gate, a drain and a source;

f) a first NFET, the first NFET having a gate, a drain and a source;

g) a second NFET, the second NFET having a gate, a drain and a source;

h) a third NFET, the third NFET having a gate, a drain and a source;

i) a fourth NFET, the fourth NFET having a gate, a drain and a source;

j) a fifth NFET, the fifth NFET having a gate, a drain and a source;

k) wherein the sources of the first, second, and third PFETs are connected to VDD;

l) wherein the sources of the first, second, and third NFETs are connected to GND;

m) wherein the drains of the fourth PFET, the fifth PFET, the fourth NFET, and the fifth NFET are connected to the output of the forward inverter/majority voter;

n) wherein the gates of the first PFET, the second PFET, the first NFET, and the second NFET are connected to the output of the first feedback inverter;

o) wherein the gates of the third PFET, the fourth PFET, the third NFET, and the fourth NFET are connected to the output of the second feedback inverter;

p) wherein the gates of the fifth PFET and the fifth NFET are connected to the output of the third feedback inverter;

q) wherein the drain of the first PFET is connected to the source of the fourth PFET;

r) wherein the drain of the second PFET and the drain of the third PFET are connected to the source of the fifth PFET;

s) wherein the drain of the first NFET is connected to the source of the fourth NFET;

t) wherein the drain of the second NFET and the drain of the third NFET are connected to the source of the fifth PFET.

10) The triple redundant latch as in Claim 1 wherein the output driver comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the source of the PFET is connected to VDD;

d) wherein the source of the NFET is connected to GND;

e) wherein the gates of the NFET and the PFET are the input of the output driver;

f) wherein the drains of the NFET and the PFET are the output of the output driver.

11) A method of manufacturing a triple redundant latch with improved soft error rate comprising:

a) fabricating an input driver, the input driver having an input and an output;

b) fabricating a first transfer gate, the first transfer gate having an input, a first control input, a second control input and an output;

c) fabricating a second transfer gate, the second transfer gate having an input, a first control input, a second control input, and an output;

d) fabricating a third transfer gate, the third transfer gate having an input, a first control input, a second control input, and an output;

e) fabricating a first feedback inverter, the first feedback inverter having an input and an output;

f) fabricating a second feedback inverter, the second feedback inverter having an input and an output;

g) fabricating a third feedback inverter, the third feedback inverter having an input and an output;

h) fabricating a forward inverter/majority voter, the forward inverter/majority voter having a first input, a second input, a third input and an output;

i) fabricating an output driver, the output driver having an input and an output;

j) wherein the input of the input driver is the input of the triple redundant latch;

k) wherein the output of the input driver is connected to the input of the first transfer gate, the input of the second transfer gate, and the input of the third transfer gate;

l) wherein a first control input of the triple redundant latch is connected to the first control input of the first transfer gate, the first control input of the second transfer gate, and the first control input of the third transfer gate;

m) wherein a second control input of the triple redundant latch is connected to the second control input of the first transfer gate, the second control input of the second transfer gate, and the second control input of the third transfer gate;

n) wherein the output of the first transfer gate is connected to the output of the first feedback inverter and to the first input of the forward inverter/majority voter;

o) wherein the output of the second transfer gate is connected to the output of the second feedback inverter and to the second input of the forward inverter/majority voter;

p) wherein the output of the third transfer gate is connected to the output of the third feedback inverter and to the third input of the forward inverter/majority voter;

q) wherein the output of the forward inverter/majority voter is connected to the input of the first feedback inverter, the input of the second feedback inverter, the input of the third feedback inverter, and to the input of the output driver;

r) wherein the output of the output driver is the output of the triple redundant latch.

12) The method of manufacturing a triple redundant latch as in Claim 11 wherein the input driver comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the source of the PFET is connected to VDD;

d) wherein the source of the NFET is connected to GND;

e) wherein the gates of the NFET and the PFET are the input of the input driver;

f) wherein the drains of the NFET and the PFET are the output of the input driver.

13) The method of manufacturing a triple redundant latch as in Claim 11 wherein the first transfer gate comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the drains of the PFET and the NFET are connected to the input of the first transfer gate;

d) wherein the sources of the PFET and the NFET are connected to the output of the first transfer gate;

e) wherein the gate of the NFET is connected to the first control input of the first transfer gate;

f) wherein the gate of the PFET is connected to the second control input of the first transfer gate.

14) The method of manufacturing a triple redundant latch as in Claim 11 wherein the second transfer gate comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the drains of the PFET and the NFET are connected to the input of the second transfer gate;

d) wherein the sources of the PFET and the NFET are connected to the output of the second transfer gate;

e) wherein the gate of the NFET is connected to the first control input of the second transfer gate;

f) wherein the gate of the PFET is connected to the second control input of the second transfer gate.

15) The method of manufacturing a triple redundant latch as in Claim 11 wherein the third transfer gate comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the drains of the PFET and the NFET are connected to the input of the third transfer gate;

d) wherein the sources of the PFET and the NFET are connected to the output of the third transfer gate;

e) wherein the gate of the NFET is connected to the first control input of the third transfer gate;

f) wherein the gate of the PFET is connected to the second control input of the third transfer gate.

16) The method of manufacturing a triple redundant latch as in Claim 11 wherein the first feedback inverter comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the source of the PFET is connected to VDD;

d) wherein the source of the NFET is connected to GND;

e) wherein the gate of the NFET and the gate of the PFET are the input of the first feedback inverter;

f) wherein the drain of the NFET and the drain of the PFET are the output of the first feedback inverter.

17) The method of manufacturing a triple redundant latch as in Claim 11 wherein the second feedback inverter comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the source of the PFET is connected to VDD;

d) wherein the source of the NFET is connected to GND;

e) wherein the gate of the NFET and the gate of the PFET are the input of the second feedback inverter;

f) wherein the drain of the NFET and the drain of the PFET are the output of the second feedback inverter.

18) The method of manufacturing a triple redundant latch as in Claim 11 wherein the third feedback inverter comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the source of the PFET is connected to VDD;

d) wherein the source of the NFET is connected to GND;

e) wherein the gate of the NFET and the gate of the PFET are the input of the third feedback inverter;

f) wherein the drain of the NFET and the drain of the PFET are the output of the third feedback inverter.

19) The method of manufacturing a triple redundant latch as in Claim 11 wherein the forward inverter/majority voter comprises:

a) a first PFET, the first PFET having a gate, a drain and a source;

b) a second PFET, the second PFET having a gate, a drain and a source;

c) a third PFET, the third PFET having a gate, a drain and a source;

d) a fourth PFET, the fourth PFET having a gate, a drain and a source;

e) a fifth PFET, the fifth PFET having a gate, a drain and a source;

f) a first NFET, the first NFET having a gate, a drain and a source;

g) a second NFET, the second NFET having a gate, a drain and a source;

h) a third NFET, the third NFET having a gate, a drain and a source;

i) a fourth NFET, the fourth NFET having a gate, a drain and a source;

j) a fifth NFET, the fifth NFET having a gate, a drain and a source;

k) wherein the sources of the first, second, and third PFETs are connected to VDD;

l) wherein the sources of the first, second, and third NFETs are connected to GND;

m) wherein the drains of the fourth PFET, the fifth PFET, the fourth NFET, and the fifth NFET are connected to the output of the forward inverter/majority voter;

n) wherein the gates of the first PFET, the second PFET, the first NFET, and the second NFET are connected to the output of the first feedback inverter;

o) wherein the gates of the third PFET, the fourth PFET, the third NFET, and the fourth NFET are connected to the output of the second feedback inverter;

p) wherein the gates of the fifth PFET and the fifth NFET are connected to the output of the third feedback inverter;

q) wherein the drain of the first PFET is connected to the source of the fourth PFET;

r) wherein the drain of the second PFET and the drain of the third PFET are connected to the source of the fifth PFET;

s) wherein the drain of the first NFET is connected to the source of the fourth NFET;

t) wherein the drain of the second NFET and the drain of the third NFET are connected to the source of the fifth PFET.

20) The method of manufacturing a triple redundant latch as in Claim 11 wherein the output driver comprises:

a) a PFET, the PFET having a gate, a drain and a source;

b) a NFET, the NFET having a gate, a drain and a source;

c) wherein the source of the PFET is connected to VDD;

d) wherein the source of the NFET is connected to GND;

e) wherein the gates of the NFET and the PFET are the input of the first output driver;

f) wherein the drains of the NFET and the PFET are the output of the first output driver.

21) The method of manufacturing a triple redundant latch as in Claim 11 wherein the triple redundant latch is manufactured in CMOS on a semiconductor substrate.

22) The method of manufacturing a triple redundant latch as in Claim 11 wherein the triple redundant latch is manufactured in CMOS on SOI.